GDR HOWDI 2022 MEETING:
METAL-INSULATOR TRANSITION IN ANNEALED MOS_2 DEVICES

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Single-layer MoS_2 has been widely studied due to its promising electronic and optoelectronic properties, which can be efficiently tuned by electrostatic doping in a transistor configuration [1]. To consider actual applications, a perfect understanding and control of the contacts and transport regime in the devices is required [2-3]. We present a systematic study of the transport characteristics of monolayer MoS_2 as a function of electron density and temperature. High quality MoS_2 flakes are grown by CVD on a Si/SiO_2 substrate, then plasma etched into the desired shape and top-contacted with Ti/Au through electron beam lithography (Fig. 1).

More than 10 devices were studied by electrical measurements after in-situ annealing at 600 K under vacuum. The 2- and 4-probe resistance was systematically recorded as a function of temperature (down to 20 K), gate voltage and source-drain voltage. In this presentation, we will focus on the intrinsic conductivity of the MoS_2 channel (4-probe measurements). For all the devices the conductivity increases with gate voltage and the apparent threshold voltage decreases with temperature. Insulating or metallic-type temperature dependencies are observed (without the need of top-gating or high-k dielectric capping) depending on carrier density (see Fig. 2), with a transition occurring around $2x10^{12}$ cm^{-2}. The devices exhibit high mobilities at low temperature (for CVD MoS_2 on SiO_2) on the order of 200 cm^2/Vs, with a nontrivial dependence between the gate voltage and the density of occupied states above the mobility edge (*i.e*, extended states).

A detailed analysis with different models fitting these results [3,4] will be presented to clearly elucidate the dominant transport mechanism for each doping and temperature range. For low gate voltages, thermally activated and variable-range hopping transport of in-gap states explain the drastic change in threshold voltage and the insulating transport [*e.g. Ref.* 2]. For higher gate voltages, the metallic behavior is well explained by phonon and static defects scattering, in agreement with a theoretical model done through a full energy- and momentum-dependent Boltzmann transport equation [5]. All these results are consistent with other device characterization such as Raman spectroscopy. We will show that this metal-insulator transition also matches more elaborate models involving quantum phase transitions. We will tentatively discuss how this approach can be reconciliated with the previous models, which are more consistent with the temperature and mobility ranges observed.

References

[1] Radisavljevic, B et al*., Nature Nanotechnology, 3* (2011), pp. 147-150.
[2] Songang Peng et al., *Advanced Electronics Materials, 7* (2019), p. 1900042.
[3] Byoung Hee Moon et al., *Nature Communications, 9* (2018), p. 2052 .
[4] S. Das Sarma and E. H. Hwang, *Scientific Reports, 5* (2015), p. 16655.
[5] T. Sohier et al., Physical Review Materials, 2 (2018), p. 114010

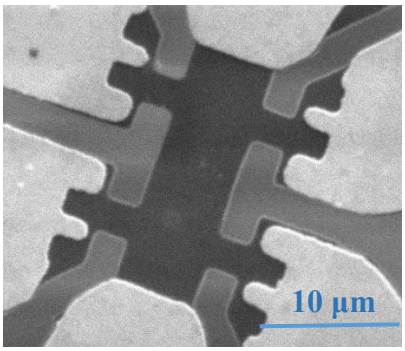

Figure 1: SEM Image of a typical device in Hall bar shape (MoS_2, SiO_2 and Au from dark to light gray).

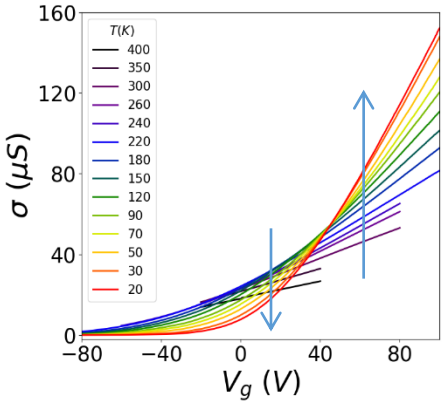

Figure 2: Typical conductivity versus gate voltage characteristic. One can notice that the conductivity increases with gate voltage (conductivity band doping), and either increases or decreases with temperature, corresponding to what is typically called a metallic or insulating behavior respectively.

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